UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,784	02/23/2004	Jong-Hyuk Baek	P-0646	5504

34610 7590 04/05/2005

FLESHNER & KIM, LLP
P.O. BOX 221200
CHANTILLY, VA 20153

EXAMINER	
COX, CASSANDRA F	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/782,784	BAEK, JONG-HYUK	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/23/04, 8/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on page 9 of the specification, in the last line on the page, the reference number "90" should be changed to --70--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-6, and 8-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Mori (U.S. Patent No. 5,600,279).

In reference to claim 1, Mori discloses in Figure 10 a phase lock loop circuit comprising: a memory (19) to store control voltage (V_{D2}); and a processor (18) to load a control voltage, which corresponds to a changed channel, from the memory (19) when a system channel is changed, and to provide the control voltage (V_{D2}) to a Voltage Control Oscillator (13), see column 5, line 54 through column 6, line 48. The same applies to claims 2, 4, 8-9, 11, 15, and 19, wherein the method includes the step of setting the control voltage as an initial control voltage (this is seen to be true when the circuit initially begins operation and uses the control voltage (V_{D1})).

In reference to claim 5, Mori discloses in Figure 10 the PLL circuit further including a signal converter (16) to convert a control voltage (V_{D1}) to a digital signal and transmit the digital signal to the memory (19). The same applies to claims 6, 12, 14, and 18, wherein the signal converter for converting signals from digital to analog is seen to be D/A converter (20).

In reference to claim 10, Mori discloses in column 6, lines 22-48 that the control voltage control voltage (V_{D2}) is loaded to the VCO (13) when a system channel is changed (wherein a channel corresponds to frequency). The same applies to claims 13, 16, and 17.

In reference to claim 20, Mori discloses in Figure 10 that the circuit further comprises a frequency generator (10), a phase detector (12), a loop filter (15), and first (11) and second (14) frequency dividers.

4. Claims 1-2, 4-6, and 8-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagidaira et al. (U.S. Patent No. 5,367,269).

In reference to claim 1, Yanagidaira discloses in Figure 13 a phase lock loop circuit comprising: a memory (5) to store control voltage; and a processor (1) to load a control voltage, which corresponds to a changed channel, from the memory (5) when a system channel is changed, and to provide the control voltage to a Voltage Control Oscillator (3), see column 1, line 34 through column 2, line 20. The same applies to claims 2, 4, 8-9, 11, 15, and 19, wherein the method includes the step of setting the control voltage as an initial control voltage (this is seen to be true when the circuit

initially begins operation and uses the control voltage provided by the phase detector for phase control).

In reference to claim 5, Yanagidaira discloses in Figure 13 the PLL circuit further including a signal converter (4) to convert a control voltage to a digital signal and transmit the digital signal to the memory (5). The same applies to claims 6, 12, 14, and 18, wherein the signal converter for converting signals from digital to analog is seen to be D/A converter (6).

In reference to claim 10, Yanagidaira discloses in Figure 13 that the control voltage is loaded to the VCO (3) when a system channel is changed (wherein a channel corresponds to frequency). The same applies to claims 13, 16, and 17.

5. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki (U.S. Patent No. 5,355,098).

In reference to claim 1, Iwasaki discloses in Figure 7 a phase lock loop circuit comprising: a memory (30) to store control voltage; and a processor (50) to load a control voltage, which corresponds to a changed channel, from the memory (30) when a system channel is changed, and to provide the control voltage to a Voltage Control Oscillator (3). The same applies to claims 2, 4, 8-9, 11, 15, and 19, wherein the method includes the step of setting the control voltage as an initial control voltage (this is seen to be true when switch 41 is closed).

In reference to claim 3, Iwasaki discloses in column 6, lines 12-17 that once the control voltage of the memory (30) is provided to the VCO (3), the processor (50) cuts off a path between the memory (30) and the VCO (3), this is done by flipping switch 42.

The same applies to claim 7, wherein the signal converter is seen to be disabled by the disconnection to the VCO (3).

In reference to claim 5, Iwasaki discloses in Figure 7 the PLL circuit further including a signal converter (60) to convert a control voltage to a digital signal and transmit the digital signal to the memory (30). The same applies to claims 6, 12, 14, and 18, wherein the signal converter further converts signals from digital to analog signals using D/A converter (63).

In reference to claim 10, Iwasaki discloses in Figure 7 that the control voltage is loaded to the VCO (3) when a system channel is changed (wherein a channel corresponds to frequency). The same applies to claims 13, 16, and 17.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

April 1, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800